

[illegible]

FIG 2C

A cross-sectional view of a semiconductor device 100. The device consists of a substrate 80 with a hatched pattern. Above the substrate is a thin layer 114, followed by a thicker layer 110. The top surface of layer 110 is divided into several regions: an n^+ region (30), a p region (40), an n^- region (40), a central gate structure G2 (70, 72), another n^- region (40), and an n^+ region (50). The gate structure G2 is a vertical stack of layers 70 and 72. A contact structure 50 is located in the n^+ region (50). The top surface of the device is labeled 112. The entire structure is labeled 100.

FIG 3

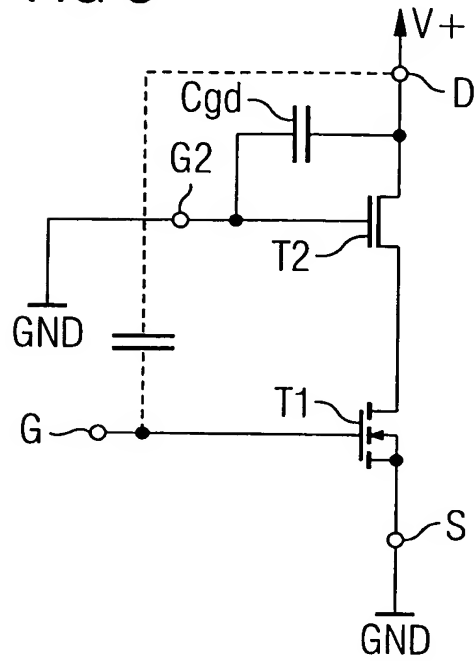


FIG 4

